Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-24. (Canceled).

25 (New). A semiconductor integrated circuit device comprising:

trenches formed in a semiconductor substrate and defining active regions and dummy regions not functioning as an element;

element isolation insulating films filled in said trenches;

first dummy interconnections formed over said substrate and not functioning as an element; and

second dummy interconnections formed over a first interlayer insulating film and not functioning as an element,

wherein said dummy regions, said first dummy interconnections and said second dummy interconnections are arranged at a scribing area,

wherein said first dummy interconnections are formed by the same level layer as a gate electrode of a memory device,

wherein said second dummy interconnection is formed by the same level layer as interconnections of said memory device.

26 (New). A semiconductor integrated circuit device according to claim 25, wherein said memory device is a dynamic random access memory.

27 (New). A semiconductor integrated circuit device according to claim 25, wherein said memory device is a dynamic random access memory including memory cells and bit lines,

wherein said memory cell includes a MISFET,

wherein said gate electrode is a gate electrode of said MISFET,

wherein said interconnections function as said bit lines.

28 (New). A semiconductor integrated circuit device according to claim 25, wherein said first dummy interconnections are formed over said dummy regions,

wherein said second dummy interconnections are formed over said first dummy interconnections.

29 (New). A semiconductor integrated circuit device comprising:

a first trench formed in a semiconductor substrate, said first trench surrounding active regions;

a second trench formed in said semiconductor substrate, said second trench surrounding dummy regions not function as an element;

element isolation insulating films filled in said first trench and said second trench;

first dummy interconnections formed over said substrate and not functioning as an element; and

second dummy interconnections formed over said first interlayer insulating film and not functioning as an element,

wherein said dummy regions, said first dummy interconnections and said second dummy interconnections are arranged at a scribing area,

wherein said first dummy interconnections are formed by the same level layer as a gate electrode of a memory device,

wherein said second dummy interconnection is formed by the same level layer as interconnections of said memory device.

30 (New). A semiconductor integrated circuit device according to claim 29, wherein said memory device is a dynamic random access memory.

31 (New). A semiconductor integrated circuit device according to claim 29, wherein said memory device is a dynamic random access memory including memory cells and bit lines,

wherein said memory cell includes a MISFET,

wherein said gate electrode is a gate electrode of said MISFET,

wherein said interconnections function as said bit lines.

32 (New). A semiconductor integrated circuit device according to claim 29, wherein said first dummy interconnections are formed over said dummy regions,

wherein said second dummy interconnections are formed over said first dummy interconnections.